Appendix

Showing changes to reissue claims from the previous version. This appendix is only for the Examiner's convenience and is not for entry.

80. (Currently Amended) A processor for operating certain data in accordance with an instruction in a program, comprising:

a first register unit ~~for holding data~~;

a second register unit ~~for holding data~~;

a sign-extending unit ~~for sign-extending data~~;

a zero extending unit ~~for zero-extending data~~,

wherein said zero-extending unit zero-extends data when the instruction designates said first register unit and said sign-extending unit sign-extends ~~said~~ data when the instruction designates said second register unit.

81. (Previously Presented) The processor of Claim 80, wherein the instruction includes a destination operand which designates one of said first register unit and said second register unit.

82. (Previously Presented) The processor of Claim 81, wherein said data is an immediate data included in the instruction.

83. (Currently Amended) A processor for operating certain data in accordance with an instruction in a program, comprising:

a first register unit ~~for holding data~~;

a second register unit ~~for holding data~~;

a sign-extending unit ~~for sign-extending data~~;

a zero-extending unit ~~for zero-extending data~~; and

an instruction decoding unit for decoding an instruction an instruction in the program to detect a first type instruction and a second type instruction, said first type instruction including an instruction to store data into said first register unit, said second type instruction including an instruction to store data into said second register unit, with said first type instruction and said second type instruction having a different destination operand to designate whether to store data into said first register unit or said second register unit;

wherein said zero-extending unit zero-extends data when a first type instruction is detected and said sign-extending unit sign-extends ~~said~~ data when a second type instruction is detected.

84. (Previously Presented) The processor of Claim 83, wherein said data is an immediate data included in the first type instruction and the second type instruction.

85. (Currently Amended) A data processing method for executing an instruction that designates one of a first register and a second register, said method comprising ~~the steps of~~:

decoding the instruction for selecting one of the first register and the second register in accordance with an operand of the decoded instruction;

zero-extending data when said decoded instruction designates the first register; and

sign-extending ~~said~~ data when said decoded instruction designates the second register.

86. (Previously Presented) The data processing method of Claim 85, wherein the operand is a destination operand which designates one of the first register and the second register.

87. (Previously Presented) The data processing method of Claim 86, wherein said data is an immediate data included in the instruction.

88. (Currently Amended) A processor for operating certain data in accordance with an instruction, comprising:

a first register unit ~~for holding data~~;

a second register unit ~~for holding data~~;

a processing unit configured to process ~~for processing at least~~ zero-extending data when the instruction designates the first register and to process ~~for processing at least~~ sign-extending data when the instruction designates the second register.

89. (Previously Presented) The processor of Claim 88, wherein the instruction includes a destination operand which designates either the first register unit or the second register unit.

90. (Previously Presented) The processor of Claim 89, wherein the data is an immediate data.

91. (Currently Amended) A data processing method for executing an instruction that designates one of a first register and a second register, said method comprising ~~the steps of~~:

decoding the instruction;

processing ~~at least~~ zero-extending data when the instruction designates the first register; and

processing ~~at least~~ sign-extending data when the instruction designates the second register.

92. (Previously Presented) The method of claim 91, wherein said instruction includes a destination operand which designates either the first register unit or the second register unit.

93. (Previously Presented) The method of claim 92, wherein said data is an immediate data.

94. (Currently Amended) The processor for executing instructions, comprising:

a first register unit ~~for holding data~~;

a second register unit ~~for holding data~~;

a first processing unit ~~for processing zero-extending data~~; and

a second processing unit ~~for processing sign-extending data~~;

wherein an instruction directs ~~can direct~~ the first processing unit to perform zero-extending when the instruction designates the first register unit and directs ~~can direct~~ the second processing unit to perform sign-extending when the instruction designates the second register unit.